

OutSys

Hardcoded Quality

RescribOS



About Us



OutSys delivers innovative carrier-grade solutions and services to implement, simplify, and speed up the integration, provisioning, management, and testing processes in the Broadband Service Providers Networks and their Information Technology Systems

Active Member of the Broadband-Forum



Solution

RescribOS

Q-in-Q S/C-VLANs

Full Matrix

ReMapper



RescribOS
is part of the
Edge & Core Network
Solution PortfoliOS



Main Features

**High Performance, Carrier-Grade,
and Cloud-Ready**

**Built on Off-the-Shelf Hardware
and**

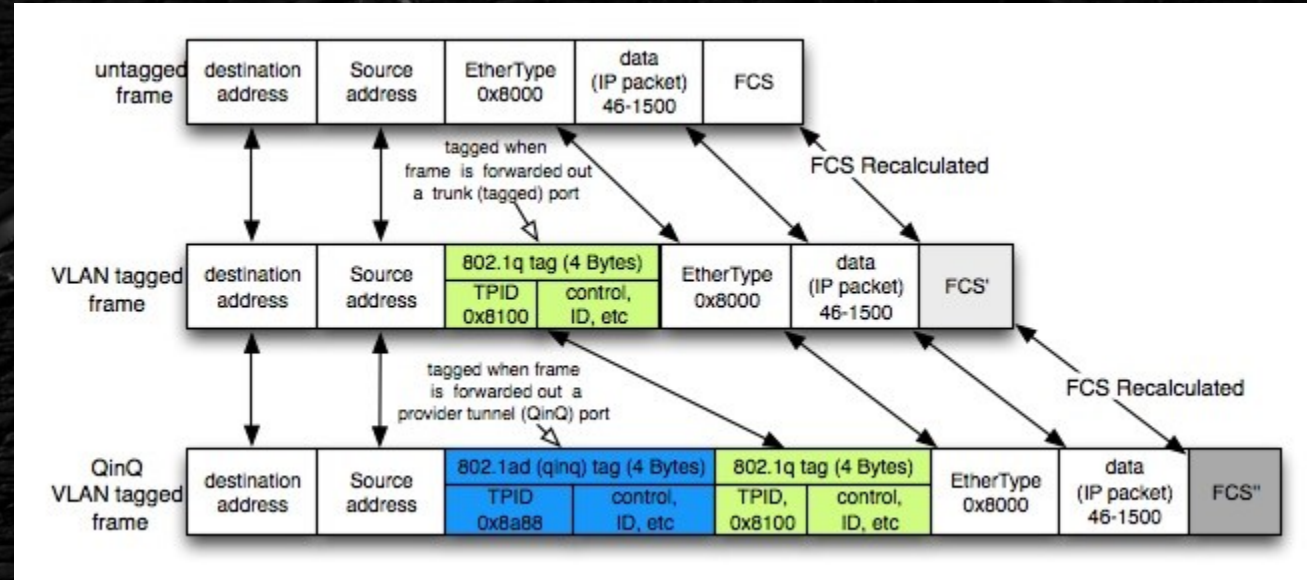
Open Software Standard Platforms

IEEE 802.3, 802.1p, 802.1q, and 802.1ad Compliant

**Easy and flexible deployment,
configuration, and management**



VLAN ReMapping



RescribOS can ReMap the full Q-in-Q S/C VLAN matrix (4096²) and ReTag the S/C Priorities



Application Areas

**Whenever a massive
VLAN ReMapping is needed**

**For instance,
at the Network Delivery Point
between a BSP Wholesaler
and its OLO Customers**



Alternatives

VLAN ReMapping can be performed by routers and switches, but with a limited number of combinations (usually around 64k~128k) due to their ASICs, Memory and CPU limitations

These restrictions make the VLAN ReMapping implementation overly complex and really difficult to manage and maintain



Competitive Advantages

**RescribOS can ReMap
the whole Q-in-Q VLAN
combination matrix
(16.777.216)
with a straightforward
implementation and
an easy management**



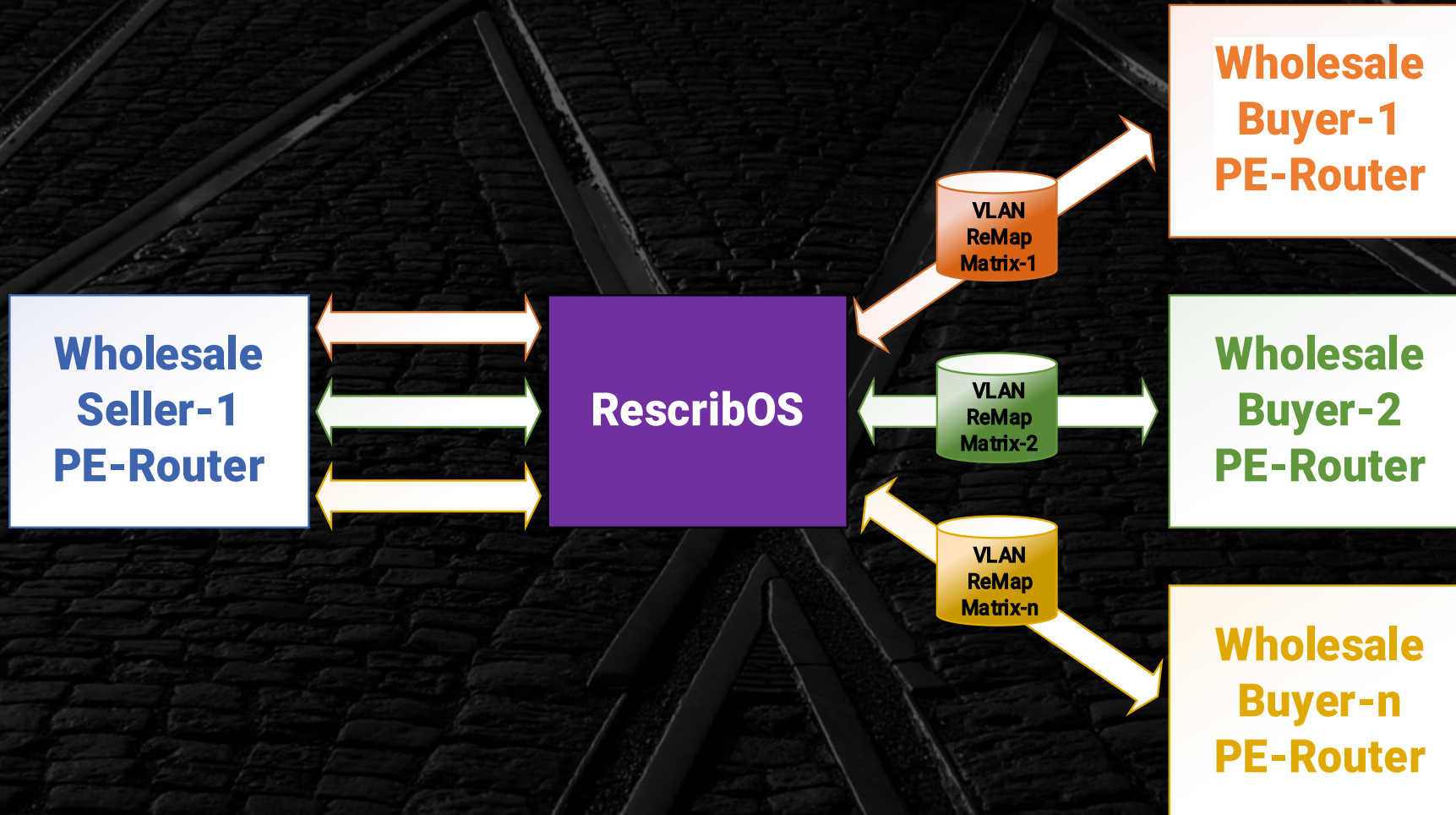
Flexibility

**Multiple Q-in-Q VLAN ReMap Matrixes
can be applied to a single RescribOS host
one every pair of network interface ports
(ingress/egress)
and/or**

**a Q-in-Q VLAN ReMap matrix can span
multiple pair of network interface ports
or even several RescribOS hosts**

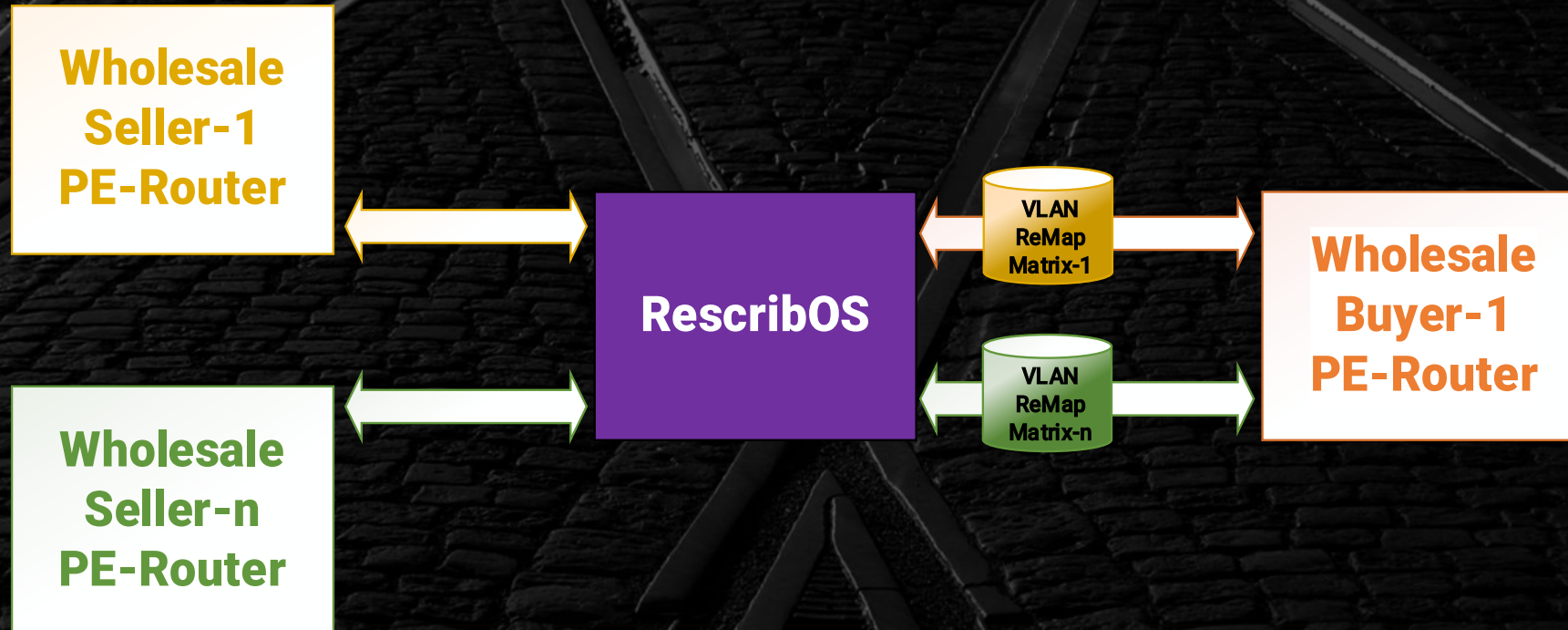


Deployment Scenario #1



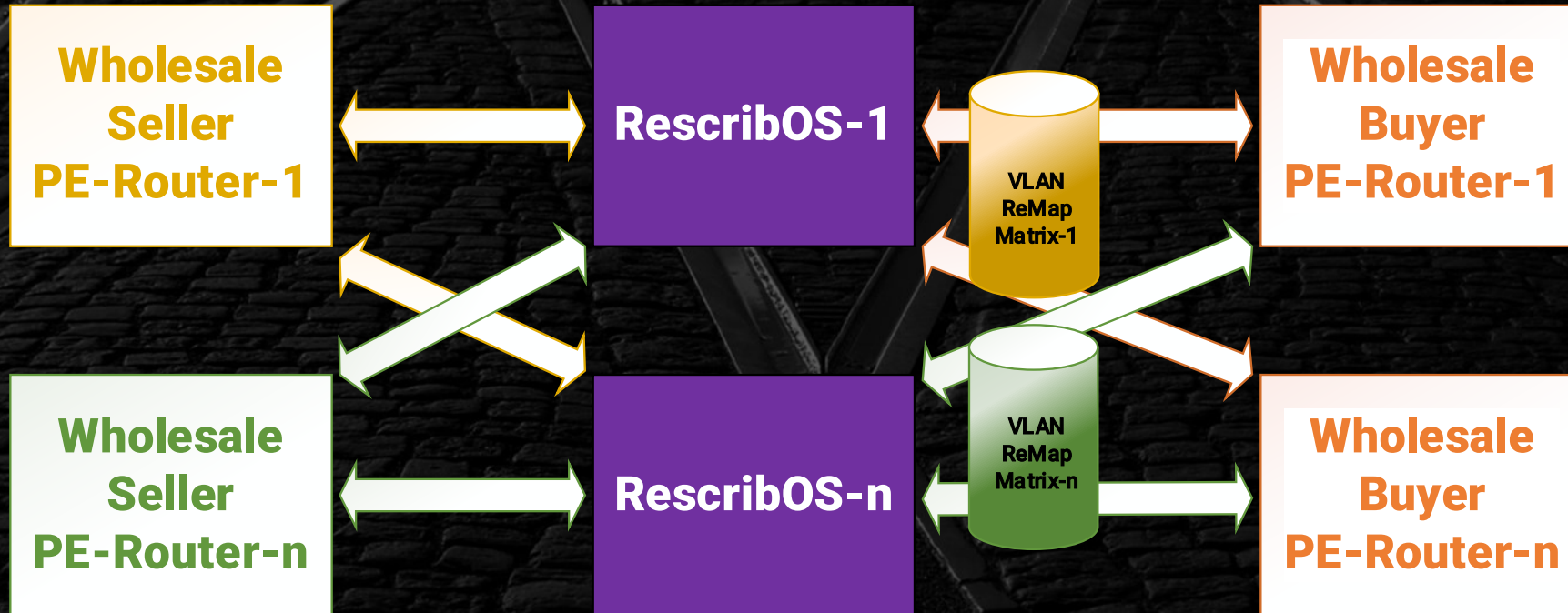


Deployment Scenario #2





Deployment Scenario HA





Control Plane

**OA&M: CLI, HTTP, SNMP
and NETCONF/RESTCONF
YANG**

Monitoring: Node Exporter

Alarms: Syslog and SNMP



User/Data Plane

**Layer 2 Ethernet:
IEEE 802.3, 802.1p, 802.1q, and 802.1ad**

**Layer 3 and Upwards:
Agnostic**



Element Manager

**Centralized Extensible
Carrier-Grade Configurator
with standard REST-APIs
for an easy seamless integration
with the BSP's OSS
infrastructure**



Performance Monitoring

**Integrated Y.1731
Frame Delay and
Synthetic Frame Loss
Measurements for
Layer-2 Performance and
Service Level Agreement (SLA)
Monitoring**



Network Softwarization

**RescribOS, leveraging on
the Network Softwarization
paradigms applied in
SDN and NVFI,
can be easily customized
to fit any BSPs needs**



Link Bonding

Straightforward Integration

**RescribOS works just like a wire
between the Routers and Switches**

**It ReMaps the VLANs without interfering
with the underlying Aggregation Protocols**



Performance

Wirespeed:

up to 200Gbit FDX on PCIe 4.0 Server
up to 400Gbit FDX on PCIe 5.0 Server



Internet Mix Size & Distribution
For each Socket/NUMA/NIC



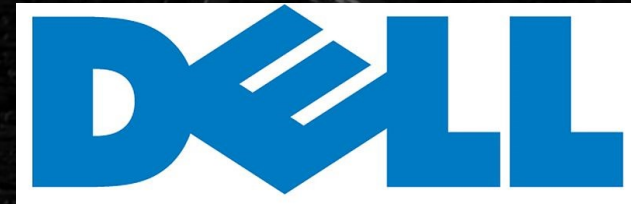
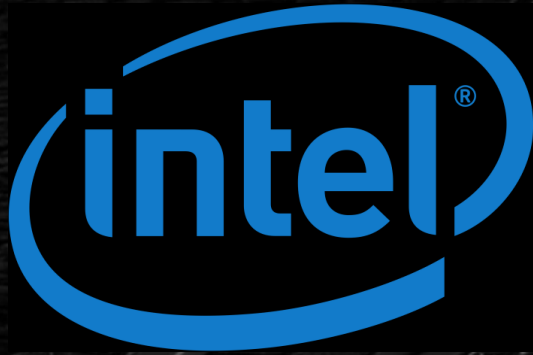
Port Combination & Density



**On a 1u, 2 Socket, PCIe 5.0 Server
several port combinations are available:
from 16x10Gbit to 2x400Gbit**



H&S Multivendor Solution





**RescribOS runs on all the
major Linux distros:**

**Red Hat, CentOS, Rocky,
SuSe, Ubuntu, Debian, etc.**

From Kernel 3.x



Data Plane Development Kit

is a set of libraries designed to accelerate packet processing workloads

It supports a broad range of Network Interface Controllers (NICs)



Cloud Ready

**Linux & DPDK are the Building Blocks
of most Network Virtualization
Environments**

**RescribOS can run as guest
on any Hypervisor that supports
SR-IOV such as: KVM, VMware ESXi etc.**



Hardware - Server

Architecture: Intel/AMD x86-64

Bus: PCIe 4.0 x16 – Memory: DDR4/3200

Bus: PCIe 5.0 x16 – Memory: DDR5/4800

Vendors: DELL, HP, SuperMicro, etc.



Hardware - NIC

**NVIDIA Mellanox Ethernet
ConnectX-6/7 - PCIe4/5
10/25/40/50/100/200/400 GbE**

**Intel Ethernet
700/800 Series NICs - PCIe3/4
10/25/40/50/100 GbE**

also Broadcom, Cisco, etc.



Future-Proof

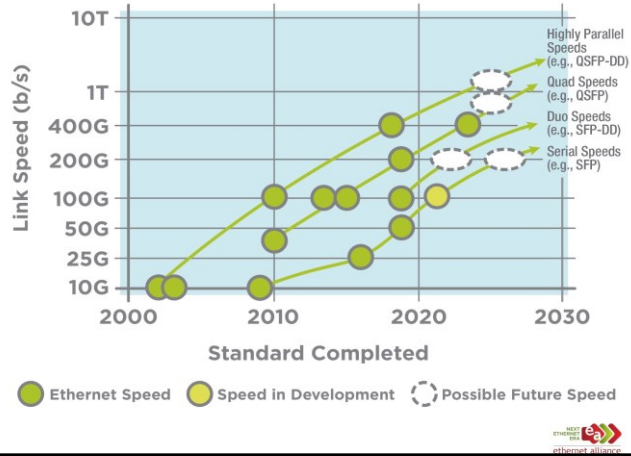
**DPDK is a
“The Linux Foundation”
project**

**Data Processing Units (DPU)
Smart NICs equipped with FPGA
are coming**

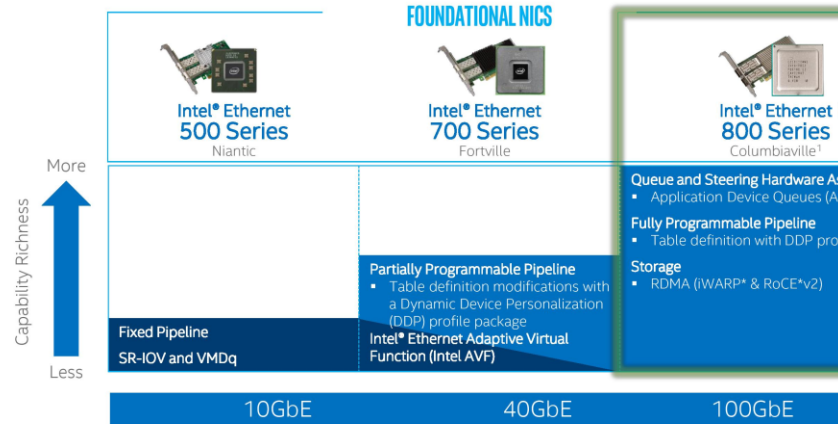


Leveraging Moore's Law

TO TERABIT SPEEDS



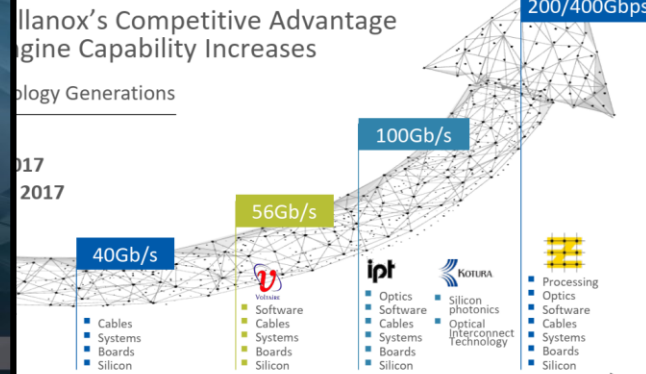
Intel® Ethernet Architecture Evolution



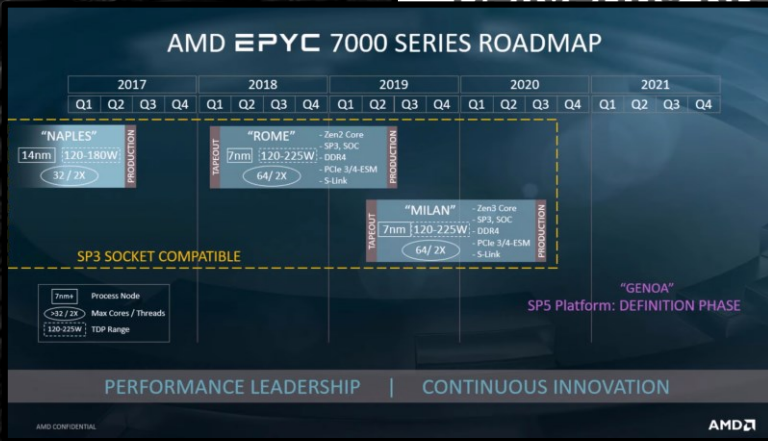
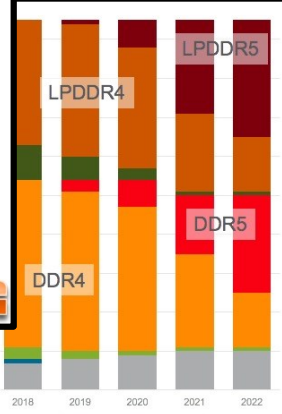
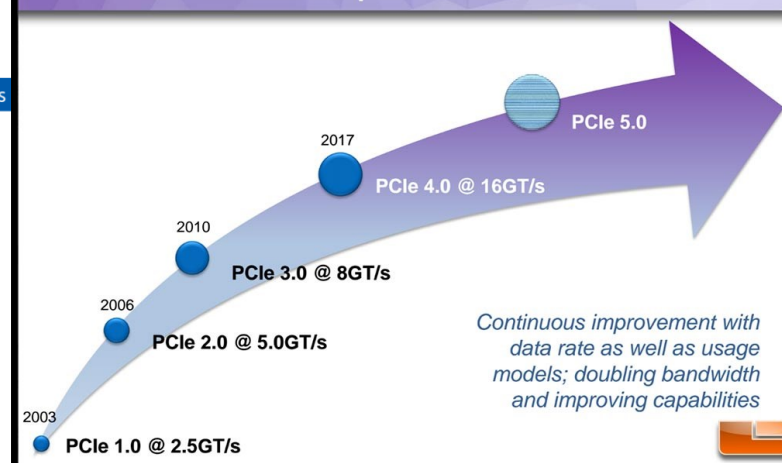
INCREASING THE PACE OF INNOVATION



Mellanox Delivering Breakthrough Technology



PCIe® Roadmap





New Hardware Readiness

**Off-the-Shelf Hardware and
Standard Software Platforms enable
the fastest integration of new hardware**

**Near Future:
Bus: PCIe 6.0 x16 – Memory: DDR6/4xxx
800GbE NIC Ports**

ARM Architecture and CPUs



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Thank You

