

The background of the entire slide is a dark grey or black field filled with a repeating pattern of overlapping, light grey circles. The circles are arranged in a grid-like fashion, with some overlapping others, creating a textured, metallic or industrial appearance.

Q OutSYS

Hardcoded Quality

EncapsOS-GRE



OutSys delivers innovative carrier-grade solutions and services to implement, simplify, and speed up the integration, provisioning, management, and testing processes in the Broadband Service Providers Networks and their Information Technology Systems

Active Member of the Broadband-Forum



Solution

EncapsOS-GRE
Generic Routing
Encapsulation
Gateway



**EncapsOS-GRE
is part of the
Edge & Core Network
Solutions PortfoliOS**



Main Features

**High Performance, Carrier-Grade,
and Cloud-Ready**

**Built on Off-the-Shelf Hardware
and**

Open Software Standard Platforms

RFC 2784, 2890 & L2 Ethernet over GRE Compliant

**Easy and flexible deployment,
configuration, and management**



Competitive Advantage

Although most of the routers can act as GRE gateway, the number of concurrent sessions is limited to few dozen since these operations are performed by the router's CPU

Due to its SDN/NVFI architecture, the concurrent GRE sessions supported by the EncapsOS-GRE are limited by the available bandwidth only



Control Plane

**OA&M: CLI, HTTP, SNMP
and NETCONF**

System & Lawful Logging: Syslog

Monitoring: Node Exporter

Alarms: Syslog, SNMP

Routing: Static, OSPF and BGP



User & Data Plane

Layer-2 Ethernet over GRE

Layer-3 GRE IPv4 Tunnels

Layer-3 GRE IPv6 Tunnels



Element Manager

**Centralized Extensible
Carrier-Grade Configurator
with standard REST-APIs
for an easy seamless integration
with the BSP's OSS
infrastructure**



Performance Monitoring

**Integrated RFC 8072
Simple Two-Way Active
Measurement Protocol
(STAMP) Reflector**

**For Performance and
Service Level Agreement (SLA)
Monitoring**



Network Softwarization

**EncapsOS-GRE, leveraging on
the Network Softwarization
paradigms applied in
SDN and NVFI,
can be easily customized
to fit any BSPs needs**



Link Bonding

**Supported Physical Link Bonding:
Transparent, IEEE 802.3AD,
Round-Robin, Active Backup,
Balance XOR, and Broadcast**



Performance

Wirespeed:

up to 200Gbit FDX on PCIe 4.0 Server
up to 400Gbit FDX on PCIe 5.0 Server



Internet Mix Size & Distribution
Per Socket/NUMA/NIC



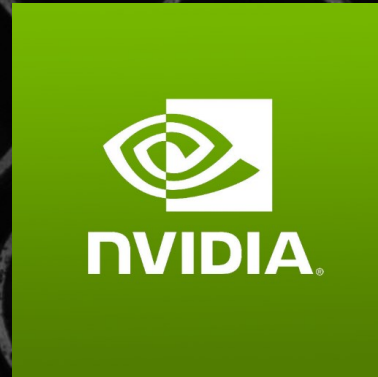
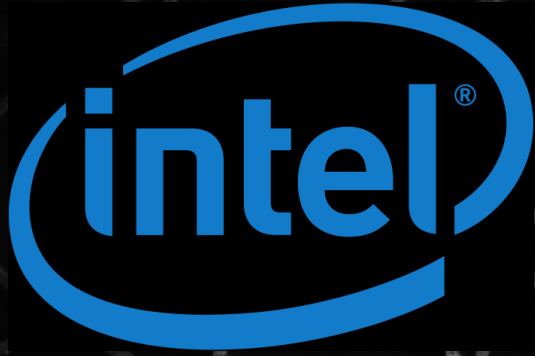
Port Combination & Density



**On a 1u, 2 Socket, PCIe 5.0 Server
several port combinations are available:
from 16x10Gbit to 2x400Gbit**



H&S Multivendor Solution





EncapsOS-GRE runs on all the major Linux distros:

**Red Hat, CentOS, Rocky,
SuSe, Ubuntu, Debian, etc.**

From Kernel 3.x



Data Plane Development Kit

**is a set of libraries designed
to accelerate packet processing
workloads**

**It supports a broad range of
Network Interface Controllers (NICs)**



Cloud Ready

**Linux & DPDK are the Building Blocks
of most Network Virtualization
Environments**

**EncapsOS-GRE can run as guest
on any Hypervisor that supports
SR-IOV such as: KVM, VMware ESXi, etc.**



Hardware - Server

Architecture: Intel/AMD x86-64

Bus: PCIe 4.0 x16 - Memory: DDR4/3200

Bus: PCIe 5.0 x16 - Memory: DDR4/4800

Vendors: DELL, HP, SuperMicro, etc.



Hardware - NIC

**NVIDIA Mellanox Ethernet
ConnectX-6/7 - PCIe4/5
10/25/40/50/100/200/400 GbE**

**Intel Ethernet
700/800 Series NICs - PCIe3/4
10/25/40/50/100 GbE**

also Broadcom, Cisco, etc.



**DPDK is a
“The Linux Foundation”
project**

**Data Processing Units (DPU)
Smart NICs equipped with FPGA
are coming**

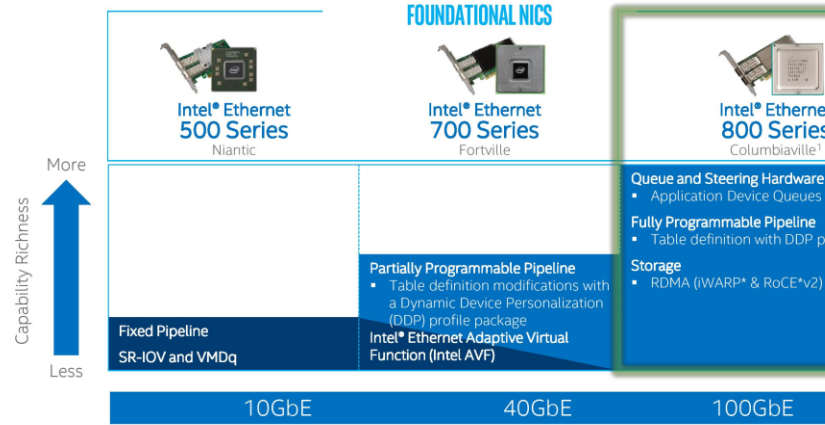


Leveraging Moore's Law

TO TERABIT SPEEDS



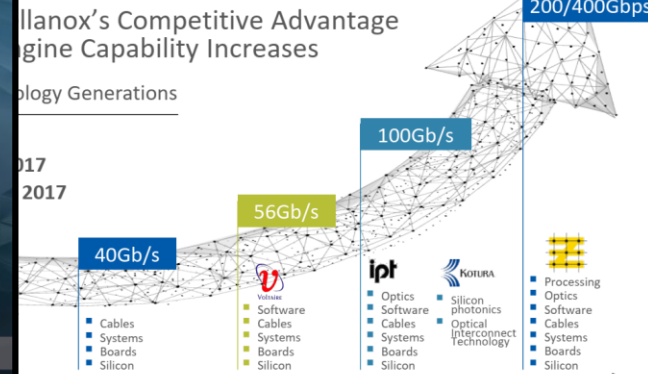
Intel® Ethernet Architecture Evolution



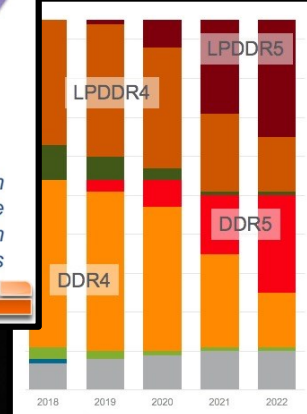
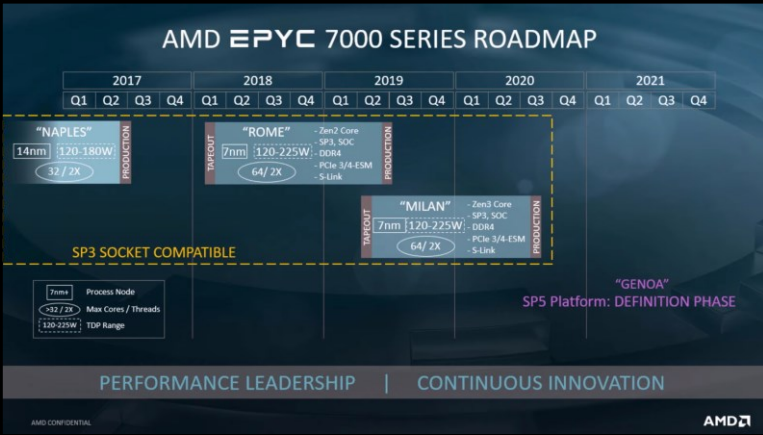
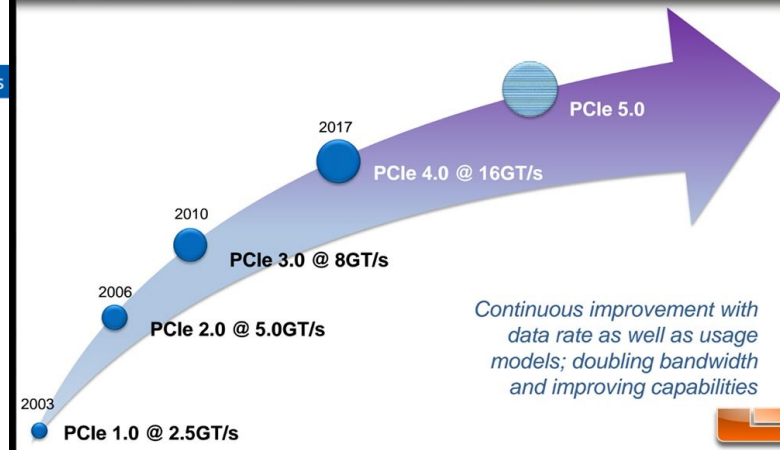
INCREASING THE PACE OF INNOVATION



Mellanox Delivering Breakthrough Technology



PCIe® Roadmap





New Hardware Readiness

**Off-the-Shelf Hardware and
Standard Software Platforms enable
the fastest integration of new hardware**

**Near Future:
Bus: PCIe 6.0 x16 – Memory: DDR6/4xxx
800GbE NIC Ports**

ARM Architecture and CPUs



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Thank You

